High Isolation, Nonreflective, GaAs, SPDT Switch, 100 MHz to 4 GHz

Data Sheet

HMC349ALP4CE

FEATURES

- Nonreflective, 50 Ω design
- High isolation: 62 dB to 2 GHz
- Low insertion loss: 1.0 dB to 2 GHz
- High input linearity
  - 1 dB power compression (P1dB): 34 dBm (typical)
  - Third-order intercept (IP3): 53 dBm (typical)
- High power handling
  - 33.5 dBm through path, V_{DD} = 5 V
  - 26.5 dBm terminated path
- Single, positive supply: 3 V to 5 V
- CMOS-/TTL-compatible control
- All off state control
- 16-lead, 4 mm × 4 mm LFCSP
- Pin-compatible with the HMC8038

APPLICATIONS

- Wireless infrastructure
- Mobile radios
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

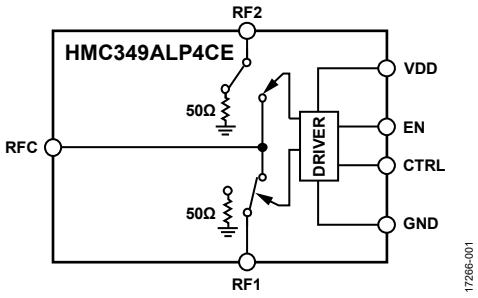

Figure 1.

GENERAL DESCRIPTION

The HMC349ALP4CE is a gallium arsenide (GaAs), single-pole, double throw (SPDT) switch, specified from 100 MHz to 4 GHz.

The HMC349ALP4CE is well suited for wireless infrastructure applications by yielding high isolation of 62 dB, low insertion loss of 1.0 dB, high input IP3 of 53 dBm, and high input P1dB of 34 dBm.

The HMC349ALP4CE operates with a single, positive supply voltage from 3 V to 5 V and provides a CMOS-/TTL-compatible control interface.

The HMC349ALP4CE comes in a 16-lead, 4 mm × 4 mm, RoHS compliant, lead frame chip scale package (LFCSP).

Rev. B

Document Feedback

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REVISION HISTORY

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

1/2019—v02.0315 to Rev. B

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Changes to Table 1 3
Deleted Bias Voltage Table and Control Voltage Table 3
Changes to Table 2 4
Added Thermal Resistance Section, Power Derating Section, and Figure 2 4
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SPECIFICATIONS

Supply voltage (V_{DD}) = 3 V to 5 V, control voltage (V_{CTRL}) = 0 V or V_{DD}, enable voltage (V_{EN}) = 0 V, case temperature (T_{CASE}) = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		4	GHz
INSERTION LOSS						
Between RFC and RF1/RF2		0.1 GHz to 1 GHz		0.9	1.2	dB
		0.1 GHz to 2 GHz		1.0	1.3	dB
		0.1 GHz to 3 GHz		1.1	1.5	dB
		0.1 GHz to 4 GHz		1.2	1.7	dB
ISOLATION						
Between RFC and RF1/RF2		0.1 GHz to 1 GHz	60	65		dB
		0.1 GHz to 2 GHz	55	62		dB
		0.1 GHz to 3 GHz	50	57		dB
		0.1 GHz to 4 GHz	50	57		dB
Between RF1 and RF2		0.1 GHz to 1 GHz		57		dB
		0.1 GHz to 2 GHz		53		dB
		0.1 GHz to 3 GHz		49		dB
		0.1 GHz to 4 GHz		46		dB
RETURN LOSS						
RFC		0.1 GHz to 1 GHz		21		dB
		0.1 GHz to 2 GHz		21		dB
		0.1 GHz to 3 GHz		17		dB
		0.1 GHz to 4 GHz		15		dB
RF1/RF2						
On		0.1 GHz to 1 GHz		21		dB
		0.1 GHz to 2 GHz		21		dB
		0.1 GHz to 3 GHz		19		dB
		0.1 GHz to 4 GHz		19		dB
Off		0.5 GHz to 1 GHz		20		dB
		0.5 GHz to 2 GHz		20		dB
		0.5 GHz to 3 GHz		17		dB
		0.5 GHz to 4 GHz		15		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		60		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		150		ns
INPUT LINEARITY[1]		300 MHz to 4 GHz				
Input 0.1 dB Power Compression	P0.1dB	V_{DD} = 3 V		25		dBm
		V_{DD} = 5 V		31		dBm
Input 1 dB Power Compression	P1dB	V_{DD} = 3 V		28		dBm
		V_{DD} = 5 V	30	34		dBm
Input Third-Order Intercept	IP3	Input power = 10 dBm/tone, Δf = 1 MHz				
		V_{DD} = 3 V		52		dBm
		V_{DD} = 5 V		53		dBm
SUPPLY INPUT		VDD pin				
Voltage	V_{DD}		3		5	V
Current	I_{DD}			1	3.5	mA
DIGITAL INPUTS		CTRL, EN pins				
Low Voltage	V_{INL}		0		0.8	V
High Voltage	V_{INH}		2		V_{DD}	V
Low Current	I_{INL}			<1		µA
High Current	I_{INH}			35		µA

[1] For input linearity performance over frequency, see Figure 14 to Figure 23.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	7 V
Digital Control Inputs	
Voltage	−1 V to V_{DD} + 1 V
Current	3 mA
RF Input Power[1, 2, 3] (f = 300 MHz to 4 GHz, T_{CASE} = 85°C)	
Through Path	
V_{DD} = 3 V	31.5 dBm
V_{DD} = 5 V	33.5 dBm
Terminated Path	
V_{DD} = 3 V to 5 V	26.5 dBm
Hot Switching	
V_{DD} = 3 V to 5 V	30 dBm
Temperature	
Junction (T_J)	150°C
Storage	−65°C to +150°C
Reflow	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	
All Pins	250 V (Class 1A)
Supply Pin	350 V

[1] For power derating at frequencies less than 300 MHz, see Figure 2.
[2] In all off state, the RFC input power handling degrades by 6 dB from through path specification.
[3] When the supply and control voltages are not powered up, RFC input power handling degrades by 6 dB from through path specification and RF1/RF2 input power handling degrades by 6 dB from terminated path specification.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-16-40		
Through Path	67.1	°C/W
Terminated Path	144.2	°C/W

POWER DERATING CURVE

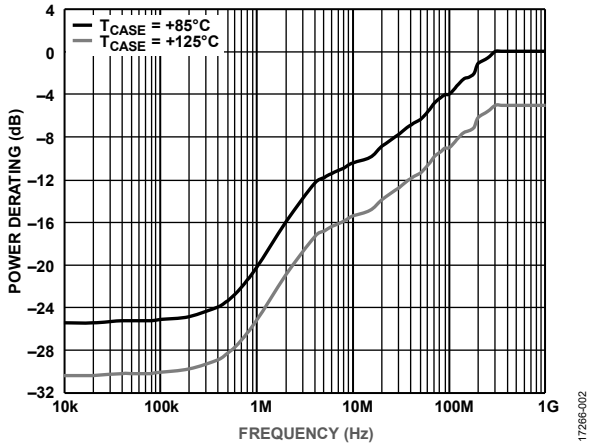

Figure 2. RF Input Power Derating

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

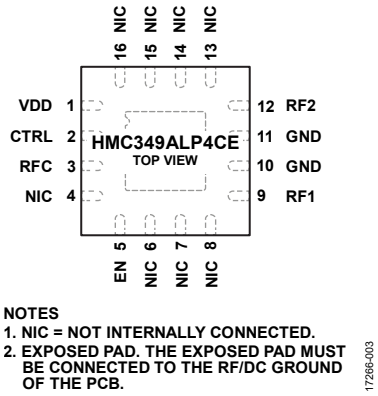

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Supply Voltage.
2	CTRL	Logic Control Input. See Table 5.
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. An external dc blocking capacitor is required on this pin.
4, 6 to 8, 13 to 16	NIC	Not Internally Connected. These pins are not connected internally.
5	EN	Logic Enable Input. See Table 5.
9	RF1	RF Throw Port 1. This pin is dc-coupled and matched to 50 Ω. An external dc blocking capacitor is required on this pin.
10, 11	GND	Ground. These pins must be connected to the RF/dc ground of the PCB.
12	RF2	RF Throw Port 2. This pin is dc-coupled and matched to 50 Ω. An external dc blocking capacitor is required on this pin.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB.

INTERFACE SCHEMATICS

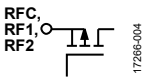

Figure 4. RFC, RF1, and RF2 Interface Schematic

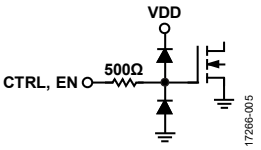

Figure 5. Digital Pins (CTRL and EN) Interface Schematic

TYPICAL PERFORMANCE CHARACTERICS

INSERTION LOSS, ISOLATION, AND RETURN LOSS

V_{DD} = 5 V, V_{CTRL} = 0 V or V_{DD}, V_{EN} = 0 V or V_{DD}, and T_{CASE} = 25°C, 50 Ω system, unless otherwise noted. Measured on the evaluation board. The board loss is subtracted for insertion loss and isolation. However, return loss includes the board effects.

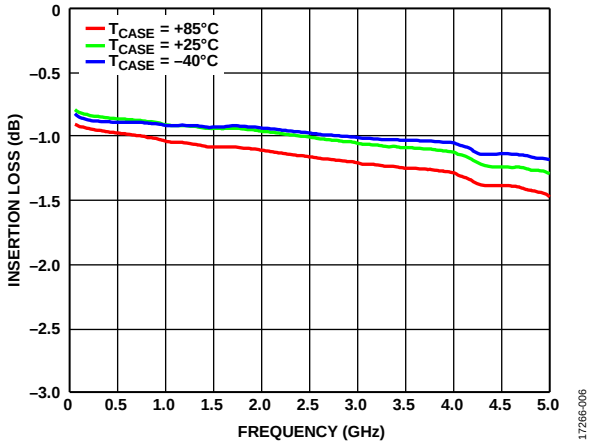

Figure 6. Insertion Loss Between RFC and RF1 vs. Frequency over Temperature

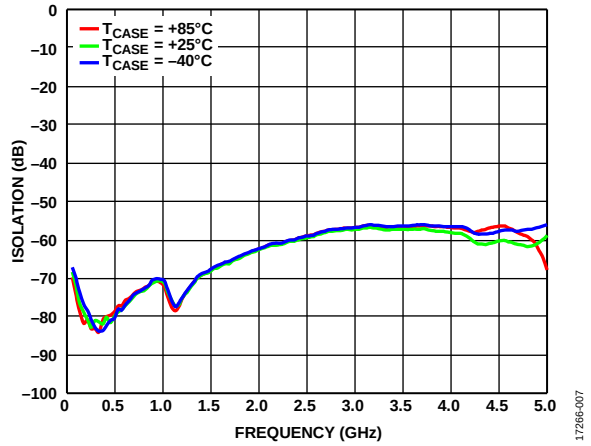

Figure 7. Isolation Between RFC and RF1 vs. Frequency over Temperature

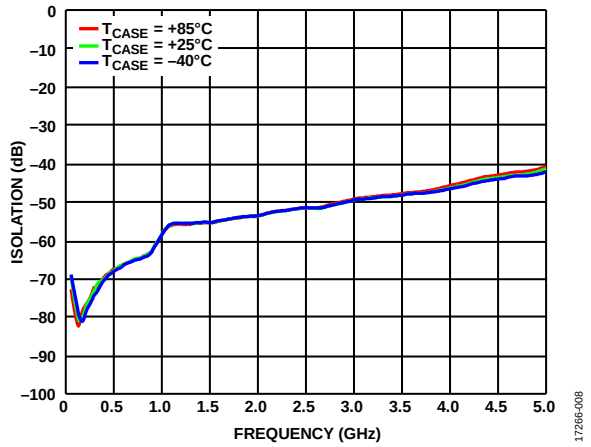

Figure 8. Isolation Between RF1 and RF2 vs. Frequency over Temperature

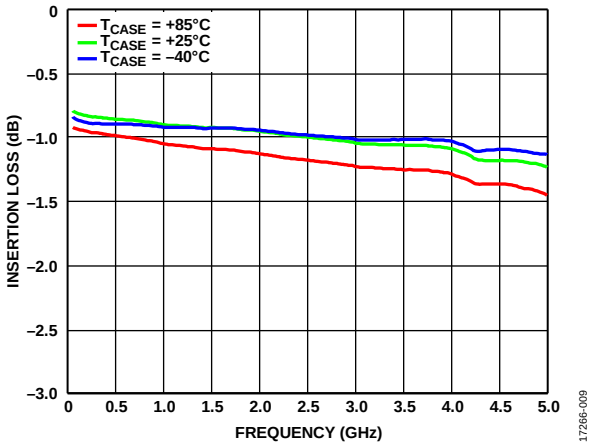

Figure 9. Insertion Loss Between RFC and RF2 vs. Frequency over Temperature

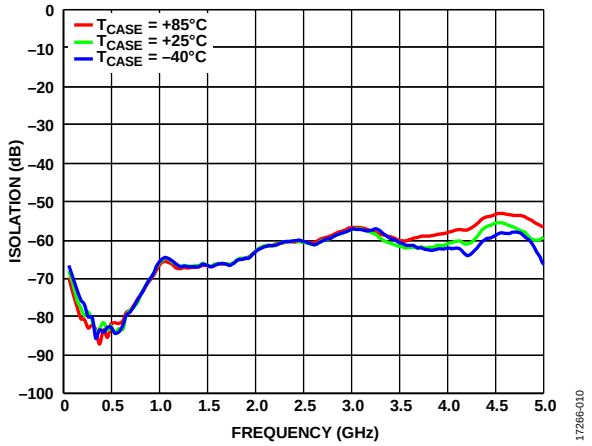

Figure 10. Isolation Between RFC and RF2 vs. Frequency over Temperature

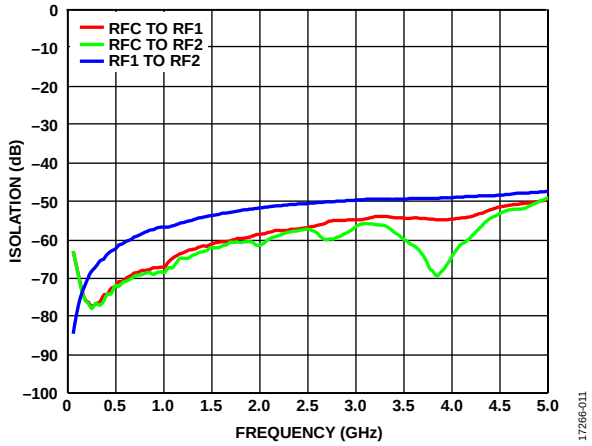

Figure 11. Isolation Between All RF Pins vs. Frequency in All Off State (EN = V_{DD})

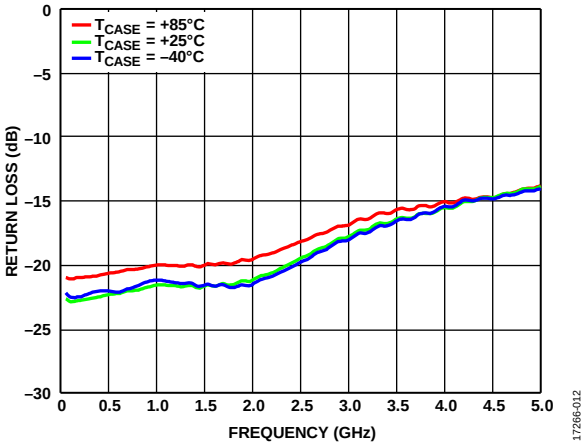

Figure 12. Return Loss for RFC vs. Frequency over Temperature

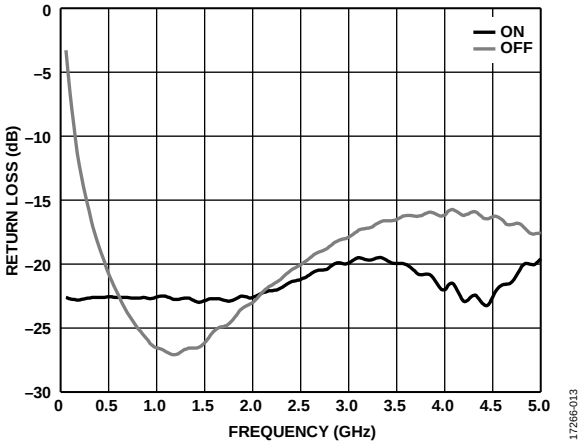

Figure 13. Return Loss for RF1 and RF2 vs. Frequency

INPUT POWER COMPRESSION AND INPUT THIRD-ORDER INTERCEPT (IP3)

V_{DD} = 3 V or 5 V, V_{CTRL} = 0 V or V_{DD}, V_{EN} = V_{DD}, and T_{CASE} = 25°C, 50 Ω system, unless otherwise noted. Measured on the evaluation board.

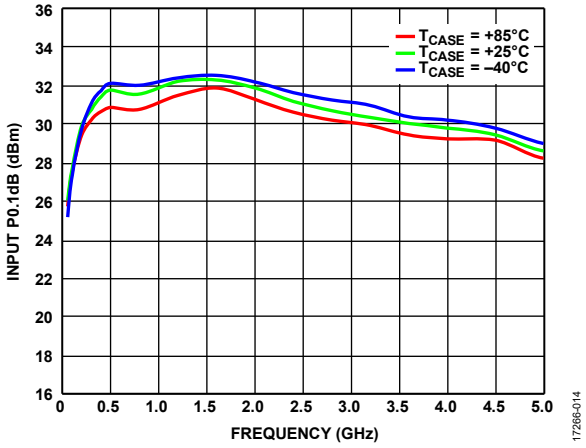

Figure 14. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Temperature, V_{DD} = 5 V

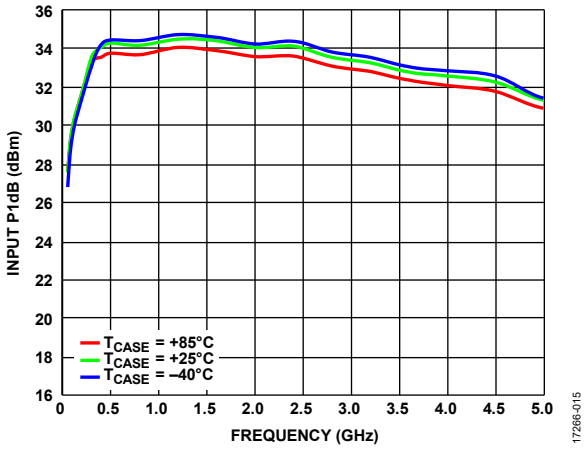

Figure 15. Input 1 dB Power Compression (P1dB) vs. Frequency over Temperature, V_{DD} = 5 V

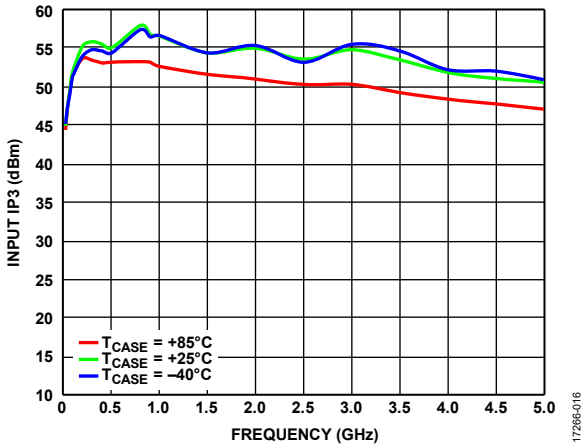

Figure 16. Input IP3 vs. Frequency over Temperature, V_{DD} = 5 V

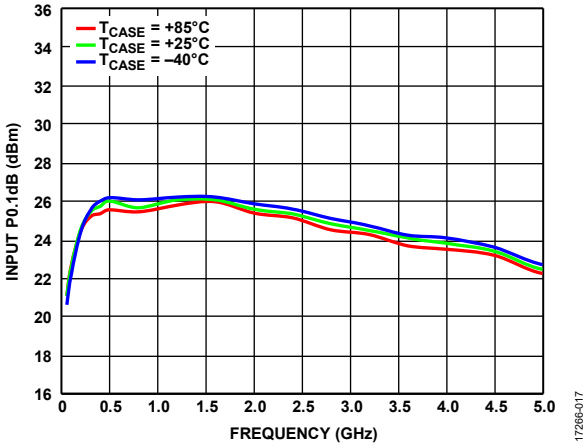

Figure 17. Input P0.1dB vs. Frequency over Temperature, V_{DD} = 3 V

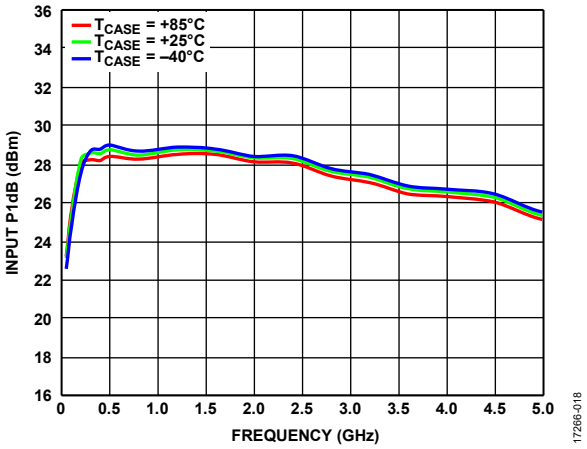

Figure 18. Input P1dB vs. Frequency over Temperature, V_{DD} = 3 V

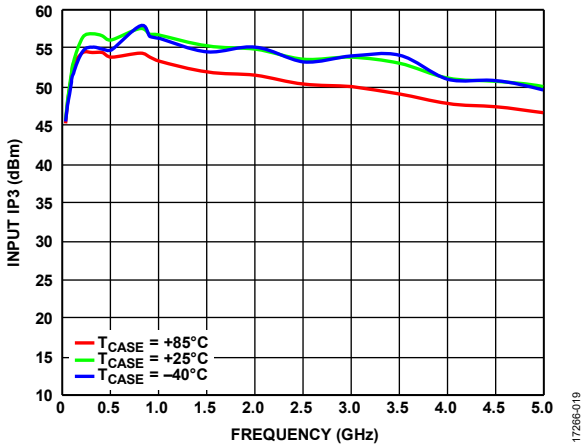

Figure 19. Input IP3 vs. Frequency over Temperature, V_{DD} = 3 V

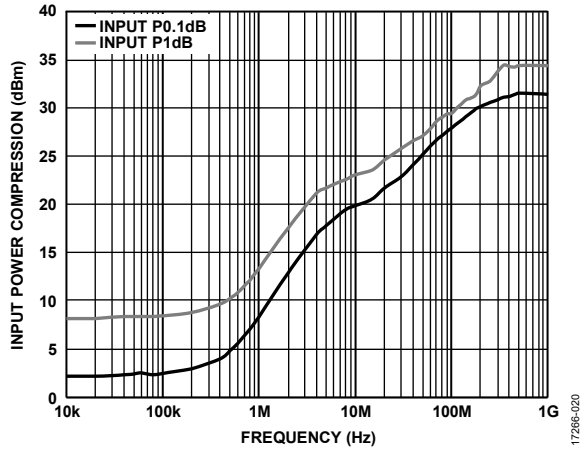

Figure 20. Input P0.1dB and Input P1dB vs. Frequency over Temperature, V_{DD} = 5 V, Low Frequency Detail

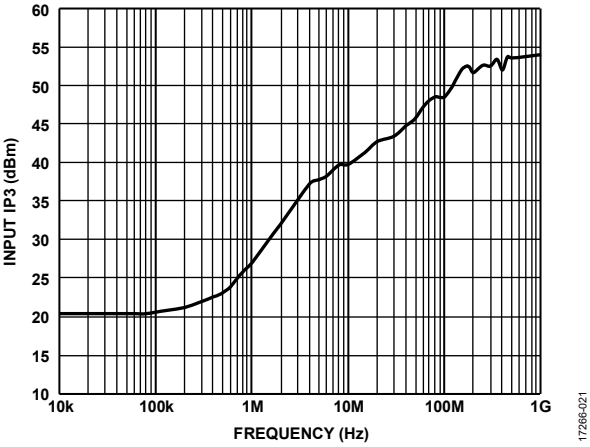

Figure 21. Input IP3 vs. Frequency over Temperature, V_{DD} = 5 V, Low Frequency Detail

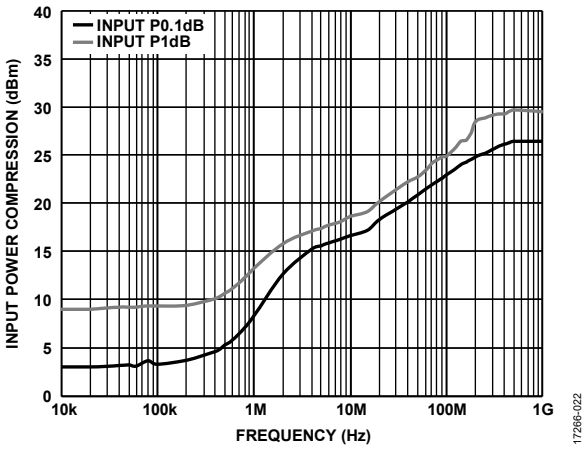

Figure 22. Input P0.1dB and Input P1dB vs. Frequency over Temperature, V_{DD} = 3 V, Low Frequency Detail

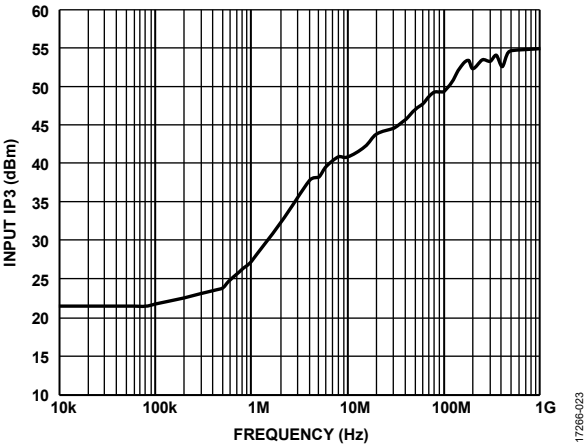

Figure 23. Input IP3 vs. Frequency over Temperature, V_{DD} = 3 V, Low Frequency Detail

THEORY OF OPERATION

The HMC349ALP4CE requires a positive supply voltage applied to the VDD pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The HMC349ALP4CE is internally matched to 50 Ω at the RF common port (RFC) and the RF throw ports (RF1 and RF2). Therefore, no external matching components are required. All RF ports are dc-coupled, and dc blocking capacitors are required at the RF ports.

The HMC349ALP4CE incorporates a driver to perform logic functions internally and to provide the user with the advantage of a simplified control interface. The driver features two digital control input pins, CTRL and EN, which control the state of the RF paths.

When the EN pin is logic low, the logic level applied to the CTRL pin determines which RF path is in the insertion loss state while the other path is in the isolation state. The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port that is terminated to an internal 50 Ω resistor.

When the EN pin is logic high, the switch is in the all off state, and both RF paths are in the isolation state regardless of the logic level applied to the CTRL. In the all off state, the RF1 and RF2 ports are terminated to internal 50 Ω resistors, and RFC becomes open reflective.

The switch design is bidirectional. The through path has same power handling whether the RF input signal is applied to the RFC port or the selected RF throw port. An RF signal can also be applied to the terminated path that has lower power handling than the through path (see Table 2).

The ideal power-up sequence is as follows:

1. VDD.
2. CTRL and EN (the relative order is not important).
3. RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 5. Control Voltage Truth Table

Digital Control Input		RF Paths	
EN	**CTRL**	**RF1 to RFC**	**RF2 to RFC**
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)
High	High	Isolation (off)	Isolation (off)

APPLICATIONS INFORMATION

EVALUATION BOARD

The HMC349ALP4CE uses a 4-layer evaluation board. The copper thickness is 0.5 oz (0.7 mil) on each layer. The top dielectric material is 10 mil Rogers RO4350, which offers good high frequency performance, and the middle and bottom dielectric materials are FR-4 type materials to achieve an overall board thickness of 62 mil. All RF and dc traces are routed on the top copper layer and the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 13 mil and ground spacing of 10 mil for a characteristic impedance of 50 Ω. For good RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Figure 24 shows the top view of the populated EV1HMC349ALP4CE evaluation board. The package ground pins are connected directly to the ground plane which is connected to the GND dc pins (J6 and J7). A single power supply port is connected to the dc pin labeled VDD (J5). An unpopulated bypass capacitor position is available to filter high frequency noise on the supply trace. Two control ports are connected to the CTRL and EN dc pins (J4 and J8). The RF ports are connected to the RFC, RF1, and RF2 connectors (J1, J3, and J2) that are PC mount subminiature version A (SMA) RF connectors. Additionally, 100 pF dc blocking capacitors (C1, C2, and C3) are used on RF transmission lines. A through transmission line that connects unpopulated RF connectors (J4 and J5) is also available to measure and remove the loss of the PCB.

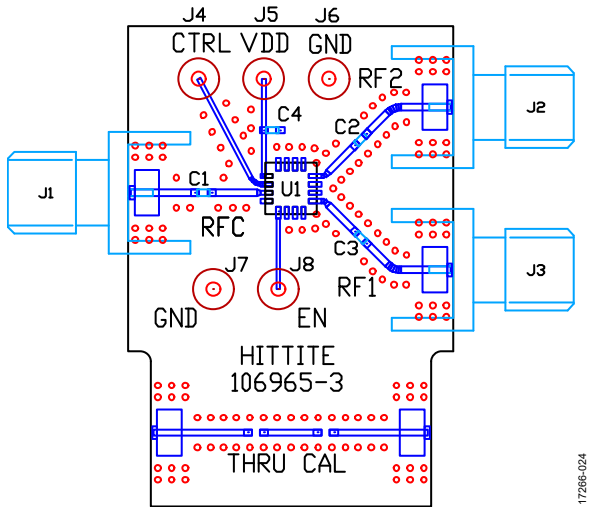

Figure 24. Populated Evaluation Board

Figure 25 and Table 6 are the evaluation board schematic and bill of materials, respectively.

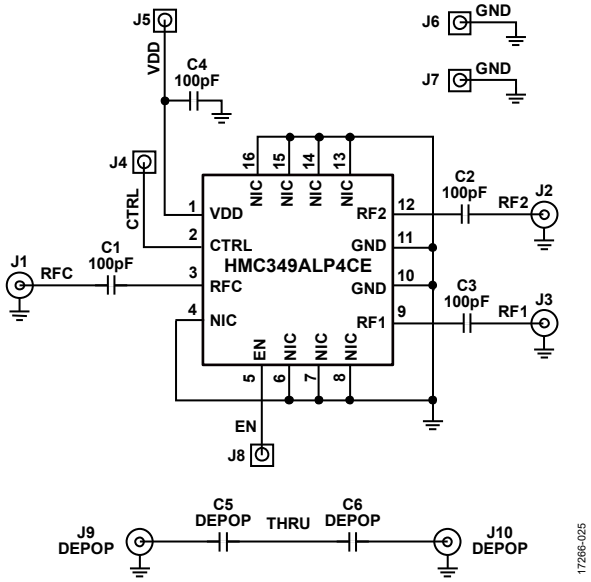

Figure 25. Evaluation Board Schematic

Table 6. Bill of Materials, Evaluation Board Components

Component	Description
J1 to J3	PC mount SMA connectors
J4 to J8	DC pins
J9, J10	PC mount SMA connectors, do not install (DNI)
C1 to C4	Capacitors, 0402 package, 100 pF
C5, C6	Capacitors, 0402 package, DNI
U1	HMC349ALP4CE SPDT switch
PCB	106965-3 evaluation PCB

OUTLINE DIMENSIONS

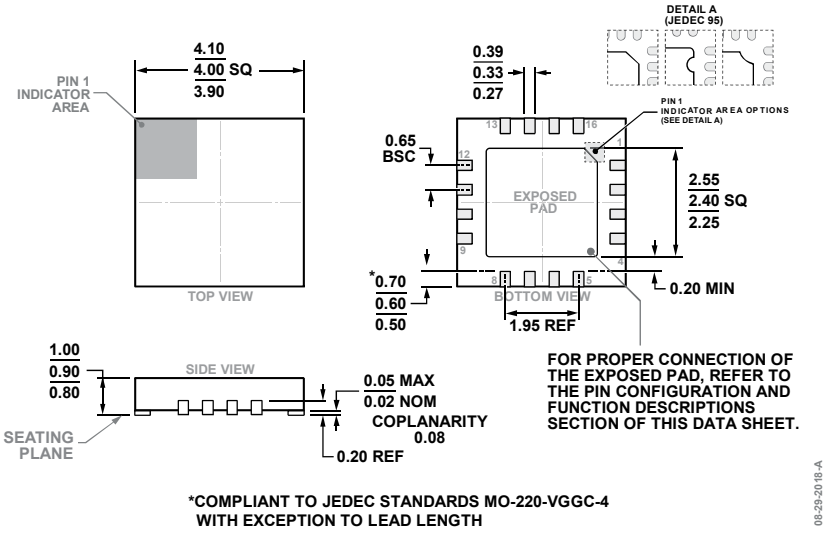

Figure 26. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.90 mm Package Height
(CP-16-40)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC349ALP4CE	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-40
HMC349ALP4CETR	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-40
EV1HMC349ALP4C		Evaluation Board	

[1] The HMC349ALP4CE, the HMC349ALP4CETR, and the EV1HMC349ALP4C are RoHS compliant parts.